What is claimed is:

1. A ferroelectric memory device, comprising:

a first bit line;

a second bit line;

a plurality of first memory cells each of which is connected to the first bit line, wherein each of the first memory cells includes one transistor and one ferroelectric capacitor;

a plurality of second memory cells each of which is connected to the second bit line, wherein each of the second memory cells includes one transistor and one ferroelectric capacitor;

a plurality of word lines each of which is connected to a respective one of the first and second memory cells;

a plurality of plate lines each of which is commonly connected to respective pairs of the first and second memory cells; and

a plurality of judgment memory cells each of which is connected between the first bit line and the second bit line, wherein each of the judgment memory cells includes two transistors and two ferroelectric capacitors.

2. The ferroelectric memory device of claim 1, further comprising a plurality of judgment word line pairs each of which is connected to a respective one of the judgment memory cell, and wherein the judgment word lines of each judgment word line pair are

supplied with a common voltage level.

3. The ferroelectric memory device of claim 1, further comprising a plurality of judgment word line pairs and a plurality of judgment plate lines each connected to respective ones of the judgment memory cells.

4. The ferroelectric memory device of claim 3, wherein each of the judgment memory cell includes:

a first transistor which has a gate electrode connected to one judgment word line of a respective judgment word line pair, a first electrode connected to the first bit line and a second electrode;

a first capacitor connected between a respective judgment plate line and the second electrode of the first transistor;

a second transistor which has a gate electrode connected to the other judgment word line of the respective judgment word line pairs, a first electrode connected to the second bit line and a second electrode; and

a second ferroelectric capacitor connected between the judgment plate line and the second electrode of the second transistor.

5. The ferroelectric memory device of claim 4, wherein each of the first memory cells includes a third transistor which has a gate electrode connected to a respective word line, a first electrode connected to the first bit line and a second electrode, and a third

capacitor connected between a respective plate line and the second electrode of the third transistor, and wherein each of the second memory cells includes a fourth transistor which has a gate electrode connected to a respective word line, a first electrode connected to the second bit line and a second electrode, and a fourth capacitor connected between the respective plate line and the second electrode of the fourth transistor.

6. The ferroelectric memory device of claim 1, further comprising a plurality digit line pairs and a plurality of gate transistor pairs, wherein each of the gate transistors pairs connects a sense amplifier to a respective digit line pair.

7. A ferroelectric memory device, comprising:

a memory cell array which includes a plurality of first ferroelectric memory cells, wherein each first memory cell has a structure of one transistor and one capacitor;

a judgment memory cell array which includes a plurality of second ferroelectric memory cells, wherein each second memory cell has a structure of two transistors and two capacitors; and

a pair of bit lines;

wherein the first memory cells in the memory cell array are alternatively connected to each bit line of the bit line pair, and wherein the second memory cells in the judgment memory cell array are connected to both bit lines of the bit line pair.

8. The ferroelectric memory device of claim 7, further comprising a plurality of

judgment word line pairs, wherein each judgment word line pair has a same voltage level, and wherein the second memory cells in the judgment memory cell array are respectively connected to the judgment word line pairs.